1. A method of evaluating the performance of a hybrid analog-digital integrated circuit having an analog unit, a digital unit, and a substrate on which the units are located, comprising:

identifying a broadband power source that represents noise characteristics of the digital unit; and

simulating performance of the integrated circuit by evaluating performance of a lumped circuit in which the source couples to a lumped element representing the substrate and the substrate couples to a lumped element representing the analog unit.

2. The method of claim 1, wherein the identifying includes evaluating one or more characteristics of the power source based on a behavioral simulation model for the digital unit.

3. The method of claim 1, further comprising:

repeating the identifying and simulating for another digital unit; and

selecting one of the two digital units based on the simulating showing that the integrated circuit has a better performance with the one of the units.

4. The method of claim 1, further comprising:

repeating the simulating for a lumped element representing another substrate; and

selecting a better one of the two substrates based on the performances determined by the acts of simulating.

5. A program storage medium encoding a computer executable program of instructions for evaluating the performance of a hybrid analog-digital integrated circuit having an analog unit, a digital unit, and a substrate on which the units are located, the instructions to cause the computer to:

identify a broadband power source that represents noise characteristics of the digital unit; and

simulate performance of the integrated circuit by evaluating performance of a lumped circuit in which the source couples to a lumped element representing the substrate and the substrate couples to a lumped element representing the analog unit.

6. The medium of claim 5, wherein the instruction to identify evaluates one or more characteristics of the power source based on a behavioral simulation model for the digital unit.

7. The medium of claim 5, wherein the instructions further cause the computer to:

repeat the identifying and simulating for another digital unit; and

select one of the two digital units based on the simulating showing that the integrated circuit has a better performance with the one of the units.

8. The medium of claim 5, wherein the instructions further cause the computer to:

repeat the simulating for a lumped element representing another substrate; and

select a better one of the two substrates based on the performances determined by the acts of simulating.

9. A method comprising:

identifying a candidate integrated circuit that comprises a candidate digital circuit;

determining a power coefficient, S_0, of said candidate digital circuit;

predicting a power spectral density, $S(\omega)$, of said candidate digital circuit based on said power coefficient, S_0, of said candidate digital circuit; and

fabricating said candidate integrated circuit when said power spectral density, $S(\omega)$, of said candidate digital circuit achieves a design goal for said candidate integrated circuit.

10. The method of claim 9 further comprising determining a mean bit rate, $\bar{\nu}$, of said candidate digital circuit, wherein said power spectral density, $S(\omega)$, of said candidate digital circuit is based on said power coefficient, S_0, and on said mean bit rate, $\bar{\nu}$.

11. The method of claim 9 wherein said candidate integrated circuit further comprises a candidate analog circuit.

12. The method of claim 11 further comprising evaluating a lumped circuit in which a noise source based on $S(\omega)$ is coupled to a multi-port network that represents a candidate substrate which is coupled to a multi-port network that represents said candidate analog circuit.

13. The method of claim 9 wherein said candidate integrated circuit comprises a plurality of candidate digital circuits.

14. The method of claim 9 wherein said power coefficient, S_0, is based on the number of switching devices composing said candidate digital circuit.

15. The method of claim 9 wherein said power coefficient, S_0, is based on the clock rate of said candidate digital circuit.

16. The method of claim 9 wherein said power coefficient, S_0, is based on a plurality of voltage levels of said candidate digital circuit.

17. The method of claim 9 wherein said power coefficient, S_0, is based on an activity factor of said candidate digital circuit.

18. A method comprising:

identifying a candidate integrated circuit that comprises a candidate digital circuit;

determining a mean bit rate, $\bar{\nu}$, of said candidate digital circuit;

predicting a power spectral density, $S(\omega)$, of said candidate digital circuit based on said mean bit rate, $\bar{\nu}$, of said candidate digital circuit; and

fabricating said candidate integrated circuit when said power spectral density, $S(\omega)$, of said candidate digital circuit achieves a design goal for said candidate integrated circuit.

19. The method of claim 18 further comprising determining a power coefficient, S_0, of said candidate digital circuit, wherein said power spectral density, $S(\omega)$, of said candidate digital circuit is based on said power coefficient, S_0, and on said mean bit rate, $\bar{\nu}$.

20. The method of claim 18 wherein said candidate integrated circuit further comprises a candidate analog circuit.

21. The method of claim 20 further comprising evaluating a lumped circuit in which a noise source based on $S(\omega)$ is coupled to a multi-port network that represents a candidate substrate which is coupled to a multi-port network that represents said candidate analog circuit.

22. The method of claim 18 wherein said candidate integrated circuit comprises a plurality of candidate digital circuits.

23. The method of claim 18 wherein said mean bit rate, $\bar{\nu}$, is based on the number of switching devices composing said candidate digital circuit.

24. The method of claim 18 wherein said mean bit rate, $\bar{\nu}$, is based on the clock rate of said candidate digital circuit.

25. The method of claim 18, wherein said mean bit rate, $\bar{\nu}$, is based on a plurality of voltage levels of said candidate digital circuit.

26. The method of claim 18 wherein said mean bit rate, $\bar{v}$, is based on an activity factor of said candidate digital circuit.